The Westinghouse High Density Microwave Packaging Program

J. A. Costello, M. Kline, F. Kuss, W. Marsh, R. Kam(1), B. Fasano (2), M. Berry (3), N. Koopman (3)

Westinghouse Electric Corporation Baltimore, Maryland

(1) TRW, Inc. Los Angeles, CA, (2) IBM Corp. East Fishkill, NY, (3) MCNC Raleigh, NC

ABSTRACT

The Westinghouse High Density Microwave Packaging (HDMP) Program investigates advanced packaging and interconnects for next generation Active Electronically Scanned Arrays (AESA's). Our teaming partners include TRW, IBM, and MCNC. The overall goal of the program is to develop appropriate designs, materials, and manufacturing processes that lead to the production of highly interconnected, very thin radar Transmit/Receive (T/R) modules with the following benefits (4:1 Cost Reduction, 10:1 Volume, Weight Reduction). Early on, interim demonstrations are planned to establish advanced packaging and interconnect processes of multiple T/R cell tiles. In the last two years of the program, these processes will be used to fabricate functional T/R cell hardware culminating with the delivery of 50 T/R cells. In this paper, the program objectives, schedule, and technologies will be reviewed.

INTRODUCTION

Active phased array radars continue to be expensive to develop and produce despite intensive development and MANTECH efforts over the last several years. Current projections from today's $2K/module cost to <$400/module in high rate production a decade from now are still too expensive for all but the most critical advanced weapon systems (1). The requirement to break through cost barriers and simultaneously achieve reductions in weight and volume is the underlying theme of the High Density Microwave Packaging (HDMP) programs.

Traditionally, array packaging has been dictated by the T/R module form factor. By integrating advanced packaging and interconnect techniques, significant reductions in T/R module size and cost can be accomplished. Figure 1 illustrates the dramatic density improvements in a coplanar array architecture versus the more traditional slat type architecture. Again, the key to

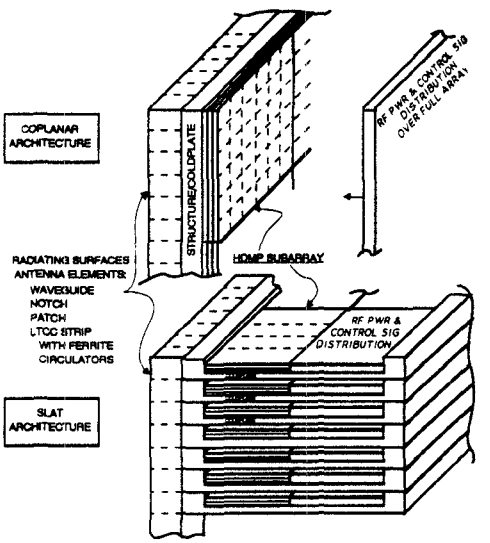

Figure 1: Array Architecture Alternatives for AESA'a

TU 3D

the coplanar approach is advanced packaging and interconnects to shrink the individual T/R cell size to meet array element spacing requirements. At X-band, this element spacing is approximately 0.6 inches square.

HDMP PACKAGE OVERVIEW

The Westinghouse HDMP packaging solution is a coplanar (tile) design based on four key elements:

* Ultra-thin, 3D, Integrated RF & Digital Packaging
* Multi-Chip, Modular RF Subarray Architecture
* Integrated CAE Tools with Module level design
* Flexible, Batch Manufacturing at All Levels with Interim Test/Rework Capabilities

The array level packaging approach is illustrated in Figure 2, including key hardware and interconnect requirements for the entire arrray. Under the HDMP program, deliverables will consist of subarray tile assemblies (Fifty T/R cells). However, functional testing of these assemblies will be limited to a microwave test

bench. Currently, 2x2 tile assembly arrays will be designed and fabricated (4 T/R cells per tile).

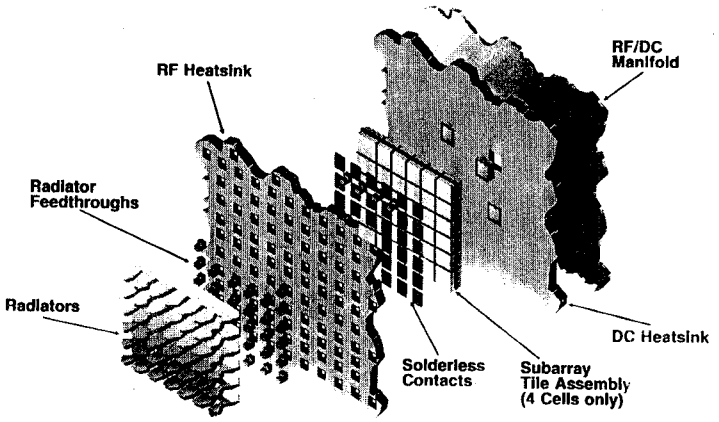

Figure 2: HDMP Array Packaging

Three dimensional packaging is necessary to maintain T/R cell spacing requirements within the array. A cross-sectional view of the of the HDMP stackup is shown in Figure 3. DC and RF components are packaged seperately on DC and RF Assembly tiles layers. Each Assembly is comprised of carrier and housing substrates. The tile assemblies are electrically interconnected with a Solder Free Interconnect (Button Board) layer which provides a microwave compatible vertical interconnection as well as a compliant, mechanical interface.

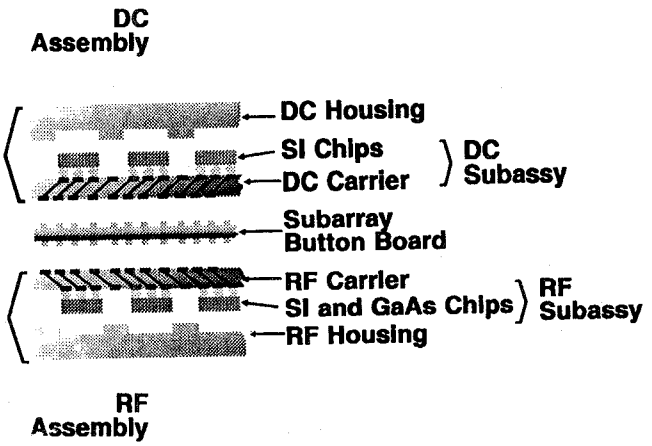

Figure 3: Cross Section View of HDMP Tile

Figure 4 illustrates the assembly process flow for the HDMP tile packaging process. The first step is to qualify all components and substrates as known good hardware. Next, active and passive components are flip chip attached to the carrier substrates. Interim DC/RF testing of this subassembly is performed. Single die removal techniques are used to replace non-functional components. With known good subassemblies, the housing substrate is then attached to complete the RF and DC Assembly tiles. Interim testing is again performed at this time. However, now, there is no possibility for assembly repair. Yields should remain quite high using pre-tested hardware and high yield assembly processing. Functional RF and DC assembly tiles are now interconnected, using the SFI technology. Electrical connection is established without heat when buttons within the SFI button board are compressed and load maintained. Functional testing of the T/R cells is then performed using a mix of probe cards and SFI interconnects.

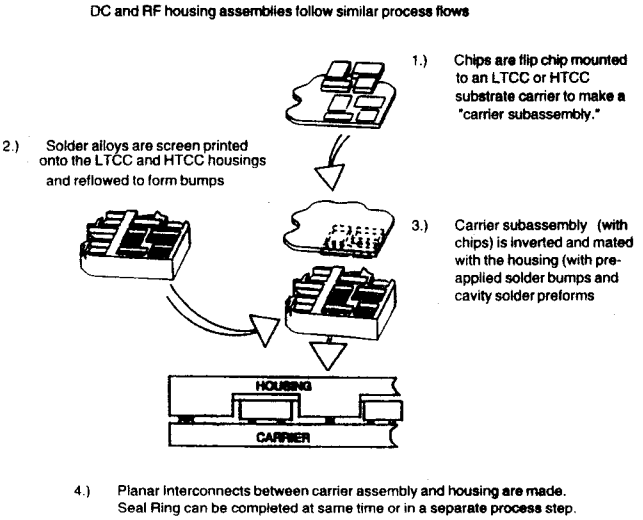

Figure 4: DC and RF Assembly Process Flow

KEY HDMP TECHNOLOGIES

Substrates: Cofired ceramics substrate technology is the foundation of the HDMP packaging approach. Both low temperature and high temperature cofired ceramic (LTCC/HTCC) systems are used. Benefits include multilayer interconnect media with controlled electrical performance, integrated passive components, stable substrates for batch processing, and integrated hermetic enclosures eliminating the need for separate housings.

For the RF assembly, where microwave performance is the key driver, an LTCC material system was chosen, owing to the enhanced dielectric properties of the glass ceramic as well as the high performance conductor

systems using gold based metals (2-4). RF loss measurements as low as 0.15 dB/in have been reported over the HDMP band. A variety of microwave transitions within the T/R cell are being developed.

The HTCC material, used for the digital side of the T/R cell, was chosen for its process maturity, mechanical strength, and compatibility with the LTCC materials. IBM is responsible for the fabrication of substrates and interconnection up to the DC assembly level. Because the microwave signals are short vertical runs through the DC assembly, microwave losses of this material are not considered an issue.

Interconnects: Three important interconnect technologies are utilized in the approach. First, flip chipping of the MMIC's and ASIC's is employed. For the DC assembly, IBM uses it's C4 process (Controlled Collaspe Chip Connection)(5). For the RF assembly, a C4-like interconnect process has been developed with MCNC for interconnecting standard GaAs MMIC's to LTCC substrates. Pb/Sn solder bumps are plated onto the LTCC carrier and the MMICs are subsequently joined. Gold ball standoffs (2-4 mils high) are being investigated to eliminate deleterious interactions between the LTCC carrier and the MMIC active surfaces. An example of a bumped die is shown in Figure 5.

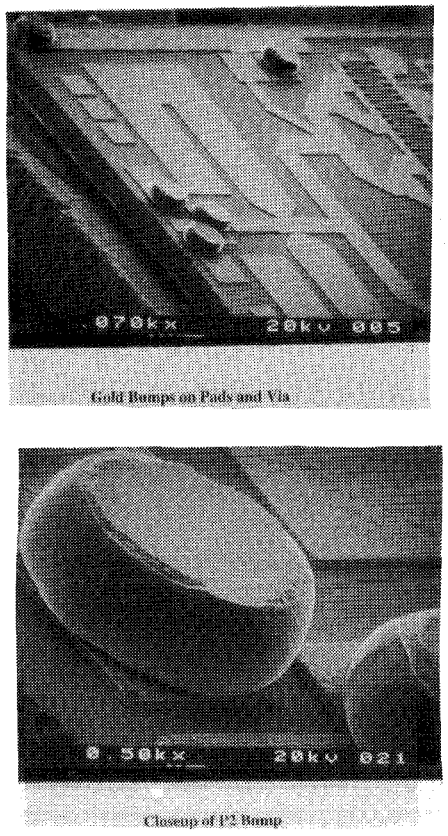

Figure 5: SEM of Au Ball Bumped MMIC

It should be noted that standard, microstrip MMICs are being used in the design (ground plane spacing of 4 mils). In addition to the standoff requirement, proper handling of RF ground at the transitions onto and off of the MMIC's and within the T/R cell is of paramount importance. RF testing of the most sensitive MMIC's in this configuration is currently under way.

The second interconnect type in the design is the carrier / housing substrate connection. For this, ceramic ball grid solder connections are used for both assemblies. Typical interconnect specifications are 20 mil solder diameters on 50 mil centers. Approximately 30-40 I/O are required within each assembly of the T/R cell.

At the same time the carrier-housing interconnects are being made, the backside chip attach to the housing substrate is also formed. The importance of this solder joint, key to the entire HDMP approach, is two fold. First, through careful volume control, this bond joint is designed to accommodate all tolerances associated with the substrates, chips, shims, etc. Detailed tolerance studies have estimated a bond joint of +/- 4 mils is sufficient for the RMS tolerance error budget. Detailed mechanical stress analyses of the solder joints will be performed since both surfaces of the MMIC are now fixed, where conventionally only the top one is.

The other key element to this interconnect step is the thermal aspect. Even with the devices flip-chipped to the carrier, a conventional thermal path is used, through the backside of the thinned chip. Solder, because of it's high conductivity, is used for the attachment. Thermal modeling results of this stackup, including thermal vias in the LTCC, indicated adequate thermal performance for all devices, even the 5W power amplifiers.

The third interconnection technology used is solder free interconnects (SFI) for vertical interconnection of the DC and RF assemblies. This technology commonly referred to as button board technology relies on very compliant single strand wire bundles within an organic dielectric substrate. Typical grid spacings include 20 mil pads on 50 mil centers. The buttons require a minimum of 3-4 oz. per contact be maintained to effect a reliable connection. Electrical contact is established with a minimum button deflection of 4 mils. Even under full compression, the button remains in the elastic range permitting it to respond to dimensional changes due to temperature excursion or vibration. Westinghouse has used this technology on a fielded digital MCM system and is currently applying it to a number of microwave MCM systems under development.

HDMP Chip Set: While the primary goal of the HDMP program is to demonstrate the advanced packaging and interconnect technologies, a chip set was chosen to

provide performance specifications that are consistent with current and future insertion designs. Performance specifications of the T/R cell are listed in Table 1.

Most MMIC's and ASIC's making up the HDMP chip set are standard parts, from various MMIC program foundries. As reported earlier, standard microstrip MMICs and ASICs are being used in the program, but in a flip chip configuration. Modest modifications are

Table 1: HDMP Performance Goals

Parameter	Goal
Frequency (Ghz)	7.5-10.5
Bandwidth	>30%
Peak Power Out	10 Watts
Power Added Efficiency	23%
Duty Cycle (mac.)	35%
Tx Pulse Width (max)	10 usec
Transmit Gain (typ)	21 dB
Receive Gain (typ)	15 dB
Rx Noise Figure (max)	3.5 dB
Rx Input 3rd Order Int.	+1.9 dB
Phase Control (Tx, Rx)	6 bits
Gain Control (Tx, Rx)	5 bits

necessary to provide compatibility. In volume production programs, device redesigns would optimize the interconnect layout for flip chip processing.

Testability/Reworkability: A key requirement for yielding highly complex multichip modules is to maintain a rigorous interim testability philosophy. Starting at the MMIC and Substrate level, known Good Die (KGD) techniques are applied. Next, interim testing at the subassembly level (Devices attached to Carriers) is planned. The T/R cell design is such that complete testability of the T/R cell is possible at this point. Internal test points are included within the layout to individually test specific stages of the T/R cell. Full power RF testing will most likely not be performed since the housing substrate is required for proper thermal management of the devices.

Repair techniques for bad MMIC's or ASIC's are available, similar to well documented processes in digital MCM technology. Removal of the individual die without disturbing the neighboring MMIC's is possible, followed by site redress, and attachment of the new die.

Design Tools: Enhanced design tools to perform module level designs is another key challenge of the program. TRW has been pursuing this task, leveraging CAD tool enhancements from their MMIC program. A block diagram of the HDMP CAD system is shown in Figure 6. The HDMP CAD system is built around the Cadence Analog Artist design automation framework. Electronic transfer of design information into the HP 3D simulator (HFSS) is being established. In addition, efficient links into the Westinghouse LTCC manufacturing facility are also being created through a Gerber translator. As part of the program, a library of microwave package transitions will be modeled and simulated to efficiently perform module level design.

SUMMARY

The Westinghouse HDMP program addresses significant reductions in the cost , weight, and volume of Transmit/Receive cells for active electronically scanned arrays through the use of advanced packaging and interconnect technologies. This paper overviews the program and its goals as well as briefly describes the technologies being applied.

ACKNOWLEDGMENTS

The authors would like to acknowledge the support of ARPA (Contract # F33615-93-C-1291) as well as the support and encouragement of the Government program management team including Tom Jones, Frank Lamb, and Tim Kemerley at Wright Labs and Eliot Cohen at ARPA.

REFERENCES

1. Longuemare, R.N., Def. Elects., Apr 1990, pp.63-66.
2. Gipprich, J.W. et al., 1995 IEEE MTT-S Digest.
3. Piloto, A. J. et al., 1994 ISHM Procedings, Boston, MA, pp. 318-323.
4. Brown, R.L. et al., 1994 IEEE MTT-S Digest, pp. 1727-1730.
5. Ray, S.K. et al., 1991 IEEE CHMT, pp. 772-778.

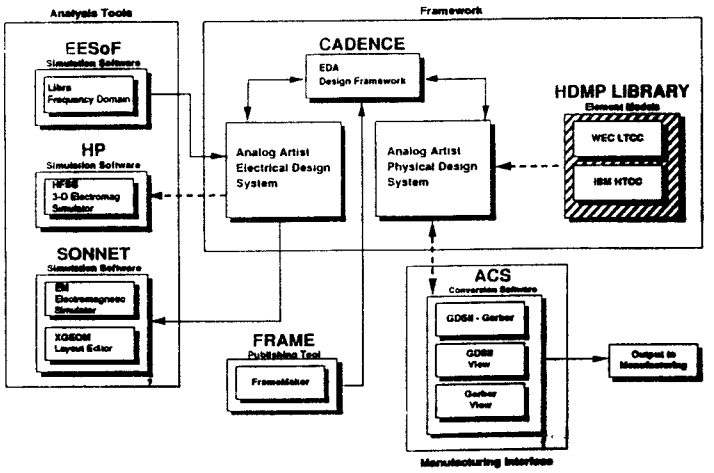

Figure 6: HDMP CAD System Block Diagram